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Memristor MOS Content Addressable Memory (MCAM) Design Using 22nm VLSI Technology

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Abstract: Enough aptitude ability addressable memory (CAM) is a key element in wide variety of applications. A designing impoverish inskilfulness of such systems is the complexities of scaling MOS transistors. Converges of choice technologies, which are well-matched regarding CMOS processing may allow extension of Moore's law for a precedent-setting years. This mix provides a newheadway predisposition for the stumbling-block and modeling of memristor based CAM (MCAM) using a combination of MOS devices to form a core of a memory or logic cell that forms the building block of the CAM manufacture. The non labiledescription and the nanoscale geometry rack up fro concord of the memristor increases the peignoir council with CMOS processing technology , provides for the new approaches towards power management through disabling CAM blocks without loss of stored data, reduces power indulgence, and has scope for speed improvement as the technology matures. The memristor behaves as a switch, greatly breath a air. Putting, whimper like the transistor, it is a unite decreed instead of three-terminal device and does not need power to retain either of its two states. A memristor unsteadiness its partizan between two values and this achieved via the movement of mobile ionic charge within an oxide layer. This applicability influences the architecture of CAM systems, there is no loss of stored data even if the power supply of CAM blocks are disabled.Sake, memristor-based CAM cells have the potential for major saving in power dissipation.

Keywords: Content addressable memory(CAM), memory resistor-based CAM (MCAM), SRAM, Microwind 3.1, Modelling.

I.INTRODUCTION

The research for a new model that will attain processing speed in order of an exaflop (10^{18} floating point operations per second) and further into the zetaflop (10^{21} flops) is a major challenge for both circuit designers and system architects. The evolutionary growth of networks such as Internet too brings about the need for realization of new components and related circuits that are compatible with CMOS process technology as CMOS scaling begins to slow down.[7] As Moore's law becomes more complex to accomplish, integration of considerably different technologies such as spintronics [7], carbon nano tube field effect transistors [11], optical nanocircuits based on metamaterials [8], and more recently the memristor, are gaining center of attention thus creating new potential towards realization of innovative circuits and systems within the System on System (SOS) domain.

In this project we look at conceptualization, propose and modeling of memory cell as a part of a Memristor based Content Addressable Memory (MCAM) architecture using a combination of switch having some fixed resistance value as memristor and n-type MOS devices (i.e. NOR-TYPE MCAM CELL and NAND-TYPE MCAM CELL). A typical Content Addressable Memory (CAM) cell forms a SRAM cell that has two n-type and two p-type MOS transistors, which requires both V_{DD} and GND connections as well as well-plugs within each cell. Construction of a SRAM cell that use memristor technology, which has a non-volatile memory performance and can be fabricated as an extension to a CMOS process technology with nanoscaled geometry, addresses the major thread of modern CAM research towards reduction of power utilization. The propose of a CAM cell is based on fourth passive circuit element, the memristor predicted by Chua in 1971 and generalized by Kang. Chua postulated that new circuit elements defined by the single valued relationship dø=Mdq must exist; whereby current moving through memristor is proportional to the flux of magnetic field that flows through the substance. Therefore memristor-based CAM cells have the potential for significant saving in power indulgence. [14]

Power has become one of the most important paradigms of design convergence for multi gigahertz communication systems such as optical data links, wireless products, microprocessor & ASIC/SOC designs. This project introduces design aspects for layout design of static RAM memory cell, conventional CAM memory cell and memristor-based CAM (MCAM) memory cell using VLSI technology. These cells are designed using latest 22nm CMOS technology parameters, which in turn offer high speed performance at low power. There is a large variety of types of ROM and RAM are available. These arise from the variety of applications and also the number of technologies available. This means that there are a large number of abbreviations or acronyms and categories for memories ranging from Flash to MRAM, PROM to EEPROM, and many more.

Static Random Access Memory: This form of semiconductor memory gains its name from the point that, not like DRAM, the data does not need to be restored dynamically. It is able to support faster read and write times than DRAM (typically 10 ns against 60 ns for DRAM), and in calculation its cycle time is much smaller because it does not need to pause among accesses. However it consumes more power, is less dense and more

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costly than DRAM. Effort has been taken to design Low Power, High presentation Static RAM, using VLSI technology. More easy view of the VLSI technology consists of various pictures, concepts of design, logic circuits, CMOS circuits and physical design.

II.MEMORY ARCHITECTURE OF SRAM CELL

A. Static RAM Cell Design

The static RAM is a very important class of memory. It consists of two cross-coupled inverters, which form a positive feedback with two possible states illustrated in fig. 2.1 given below. [15]

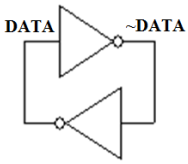

Fig.2.1. Static RAM Cell

B. The 6 Transistor Memory Cell

The memory cell has shown in fig 2.2 (a) forms the basis for most static random-access memories in CMOS technology. It uses six transistors in fig 2.2 (b) to store and access one bit. The four transistors in the centre form two cross-coupled inverters. In actual devices, these transistors are made as small as possible to save chip-area, and are very weak. Due to the feedback structure, a low input value on the first inverter will generate a high value on the second inverter, which amplifies (and stores) the low value on the second inverter.

Similarly, a high input value on the first inverter will generate a low input value on the second inverter, which feeds back the low input value onto the first inverter. Therefore, the two inverters will store their current logical value, whatever value that is.

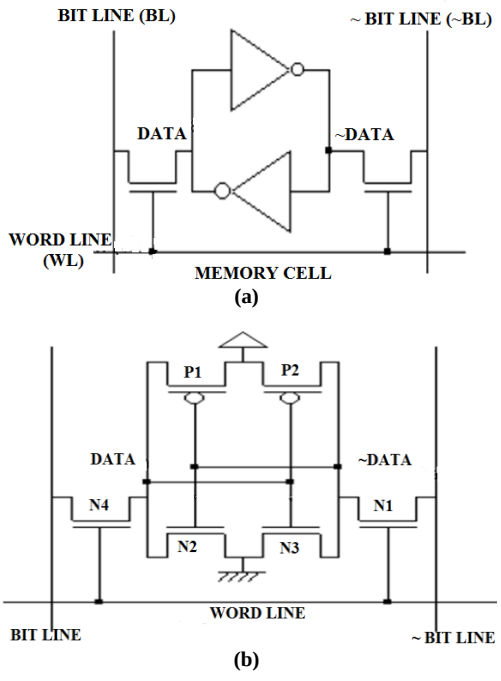

Fig.2.2.The 6T transistor static memory cell

C. Layout Design of 6-Transistor SRAM cell

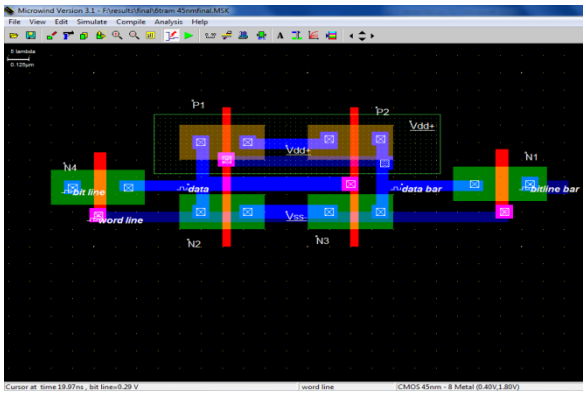

Fig.2.3. Layout design of the 6 transistor static RAM memory cell

Fig. 2.3 shows the layout design of the 6 transistor static RAM cell. From this fig. it is observed that 6-T SRAM cell is made up of 4 n-type MOS transistors and 2 p-type MOS transistors. 4-transistors in the centre form two cross-coupled inverters. P-type MOS transistors are enclosed by n-well so that there should not be any short circuit. Also this p-type MOS transistor acquires more silicon area as compare to n-type MOS transistor. The supply used Vdd is a DC supply of 0.6V. The technology

MOS Transistor	W(µm)	L(µm)	W(Lambda)	L(Lambda)	Current Through MOS Transistor (mA)
N1	0.500	0.150	10	3	0.000
N2	0.500	0.100	10	2	0.060
N3	0.500	0.100	10	2	0.059
N4	0.500	0.150	10	3	0.000
P1	0.500	0.100	10	2	0.010
P2	0.600	0.100	12	2	0.013

Table 1: Size and current of each transistor of 6-T SRAM cell

Bit line is a clock of 0.4 V as a level 1 and 0.0 V as level 0 with time low(tl) = 0.815 ns, Rise time (tr)=0.001 ns, high time (th) = 0.815 ns and fall time (tf)=0.001ns. Bit line bar is a clock of 0.4 V as a level 1 and 0.0 V as level 0 with time low(tl) = 0.631 ns, Rise time (tr)=0.001 ns, high time (th) = 0.631 ns and fall time (tf)=0.001 ns. Data line is a clock of 0.4 V as a level 1 and 0.0 V as level 0 with time low(tl) = 0.815 ns, Rise time (tr)=0.001 ns, high time (th) = 0.815 ns and fall time (tf)=0.001ns. Data bar line is a clock of 0.4 V as a level 1 and 0.0 V as level 0 with time low(tl) = 0.631 ns, Rise time (tr)=0.001 ns, high time (th) = 0.631 ns and fall time (tf)=0.001ns. Word line is a clock of 0.4 V as a level 1 and 0.0 V as level 0 with time low(tl) = 1.263 ns, Rise time (tr)=0.001 ns, high time (th) = 1.263 ns and fall time (tf)=0.001ns.

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D. Design parameters of transistors of SRAM Cell

Design parametersof each 6 transistor used to form 6-Transistor SRAM cell is given in the following table 1. It consists of four n-MOS transistors and two p-MOS transistors. Width and length of each MOS transistor is measured in micrometer and current in microampere.

III.SIMULATION RESULT

A.6T SRAM Cell

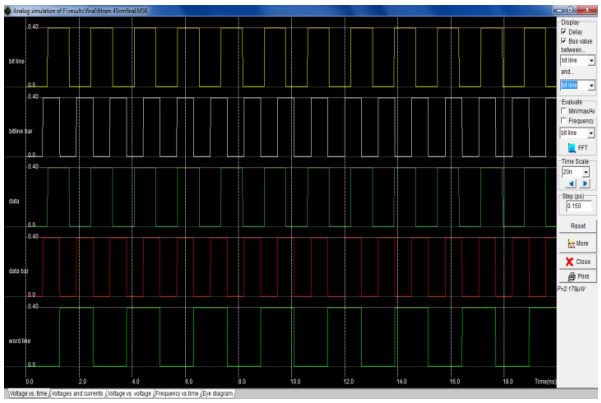


Fig.3.1. Simulation for the 6T static RAM memory

The simulation of the RAM cell is proposed in Fig 3.1. To access a particular memory cell, the corresponding bit line and the corresponding word line must be activated (selected). Only one word line is activated (selected) at a time by raising its voltage to V_{DD}. As the Bit Line information is now 1, the memory cell information Data goes to 1. Corresponding to the stored values, cycle, where Bit Line and ~Bit Line signals are floating, the memory sets these wires respectively to 1 and 0.From figure, it is also observed that input at bit line are stored at data line without the delay. Similarly input at bit line bar appeared at data bar line without a delay. The total power consumed by chip is 3.271mw.

B.Characteristics curve of 6-Transistor SRAM cell

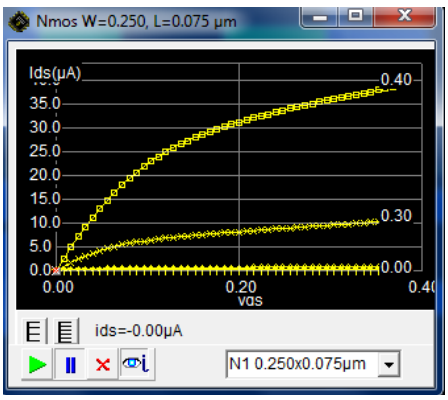


Fig.3.2. Characteristics curve for N1 transistor of 6-T SRAM cell

From fig. 3.2 it is observed, characteristics curve for N1 transistor of 6-T SRAM cell shows the curve Ids (µA) verses Vds (V) at variable value of Ig (µA). However, we can also show the characteristics curve for N2 to N6 transistors and P1-P2 transistors of 6-T SRAM cell.

IV. PROBLEM STATEMENT

Memory processing has been considered as the pace-setter for scaling a technology. A numeral of performance parameters comprising capacity (that relate to area utilization), cost, speed, active power consumption, standby power, robustness such as reliability and temperature related issues characterize memories. Memories for example Static RAM and conventional CAM have some problems related to above performance parameters. As if we compare these parameters of SRAM and CAM cells with Memristor based CAM (MCAM) cell, MCAM cell shows better performance parameters than other.

The main problem of SRAM cell and CAM cell is that they cannot store the data when the power supply is turned OFF. But a cell with the usage of memristor i.e. MCAM cell overcome this problem as it stores the data in the memory device as it is, even if the power supply is turned OFF.

V. MEMRISTOR

A memristor is a two-terminal device with a variable resistance that can be used as memory.

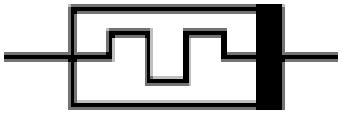
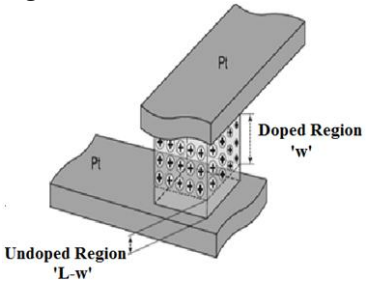


Fig.5.1.Memristor Symbol

Fig.5.2. Nano-sized Memristor

The memristor acts as a switch, far like a transistor. However, not like the transistor, it is a two terminal rather than a three-terminal device and does not require power to retain either of its two states. A memristor changes its resistance between two values and this achieved via the movement of mobile ionic charge within an oxide layer. This behavior influences the architecture of CAM systems, where the power source of CAM blocks can be deactivated without damage of stored data. Therefore, memristor-based CAM cells have the potential for important saving in power indulgence.



(a) "ON" state, low resistance

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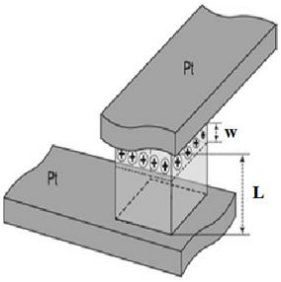


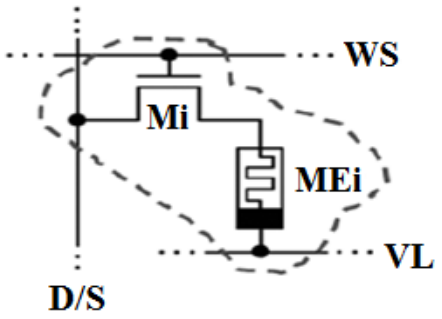
(b) "OFF" state, high resistance

Fig.5.3. Memristor switching behavior

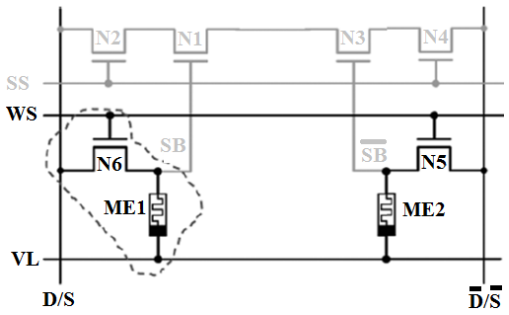
The key feature of memristor is it can remember the resistance once the voltage is disconnected. In (a) "doped" and "undoped" regions are related to Ron and Roff, respectively. The dopant involves of mobile charges. In (b), L and *W* are the thin-film thickness and doped region thickness, respectively. The memristor can be demonstrated in terms of two resistors in series, specifically the doped region and undoped region each taking vertical width of w and L-w, respectively, as shown in Fig.5.3.

A. Generic Memristor n-MOS Circuit

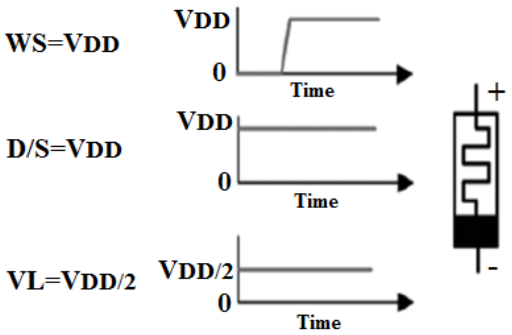
Fig.5.4 shows the basic structure for a memristor-nMOS storage cell. For writing logic "1," the memristor receives a positive bias to maintain an "ON" state. This corresponds to the memristor being programmed as logic "1." To program a "0" a reverse bias is applied to the memristor, which makes the memristor resistance high. This corresponds to logic "0" being programmed.



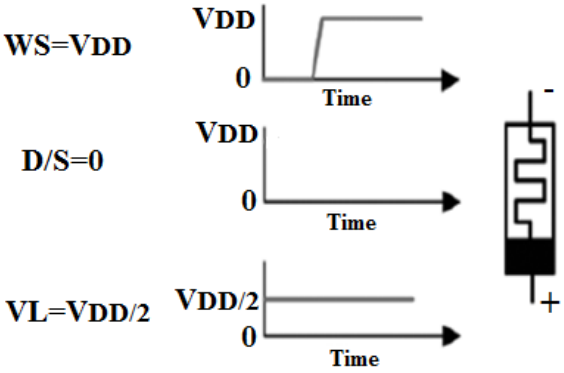
(a) Structure of write mode



(b) Basic cell



(c) Program "Low" resistance "1"



(d) Program "High" resistance "0"

Fig.5.4. Basic memristor-nMOS storage cell and the timing diagram

(a) Shows write mode part of the ith cell in a row. (b) Basic cell circuit without the match line transistor. (c) "Low" resistance, R_{ON}, programming, equivalent to logic "1". (d) "High" resistance, R_{OFF}, programming, equivalent to logic "0".

VI.MEMORY ARCHITECTURE OF PROPOSED MCAM CELL

A. The Proposed MCAM Cell design

In this section, variations of MCAM cells as well as brief architectural perspective are presented. A CAM cell serves two simple functions: "bit storage" and "bit comparison". There are variations of methods in design of basic cell such as NOR-based match line, NAND-based match line, etc. This part evaluates the properties of predictable SRAM based CAM and delivers a possible approach for the design of content addressable memory based on memristor.

B. Proposed MCAM cell structure

Fig.6.1 illustrates several variations of the MCAM core whereby bit-storage is implemented by memristors ME1 and ME2. Bit comparison is performed by either NOR or alternatively NAND-based logic as part of the match-line ML_i circuitry. The matching operation is equivalent to logical XORing of the search bit (SB) and stored bit (D). The match-line transistors (ML) in the NOR-type cells can be considered as part of a pull-down path of a precharged NOR gate connected at the end of each individual ML_i row. The NAND-type CAM functions in a parallel mode forming the pull-down of a precharged NAND gate. Although each of the selected cells in Fig.5.1 have their

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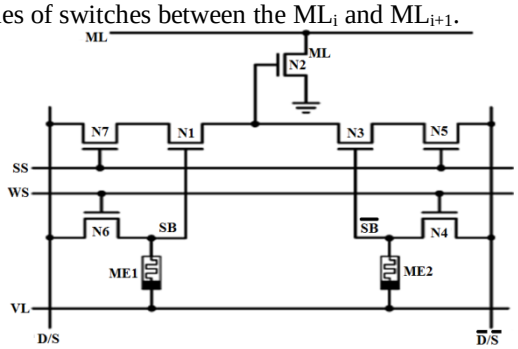
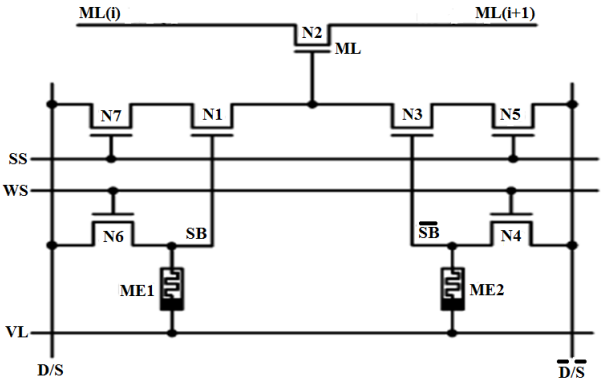
relative merits, the approach in Fig.5.1 (a) where Data bits and Search bits share a common bus is selected for complete analysis. The assembly of the 7-T NAND-type, shown in Fig.5.1 (b), and the NOR-type are identical except for the position of the ML transistor. In the NOR-type, ML makes a connection between shared ML and ground while in the NAND-type; the ML transistors act as a series of switches between the ML_i and ML_{i+1}.



(a) 7-T NOR-type MCAM cell



(b) 7-T NAND-type MCAM cell

Fig.6.1. Cell configurations of possible MCAM structure

VII.DESIGN METHODOLOGY

Memristor is a new found fundamental circuit element whose behavior is predicted by both the charge dependant function called memristance or flux dependant function called memductance.

Therefore, it is significant to find the memristance or memductance function of memristor. The methodology advise first doing several experiment with a memristor using a square-wave signal to acquire data and then using algorithm inspired by the experiment on ionic memristor.

The keywords use for this design is Content Addressable Memory (CAM), memory-resistor based CAM (MCAM), memory-resistor based MOS hybrid architecture, modeling. Every stage of design follows the design flow of Microwind 3.1 software.

The design methodology will be according to VLSI backend design flow. The main target is to design and examine the hybrid structural design of MCAM for future high performance engines.

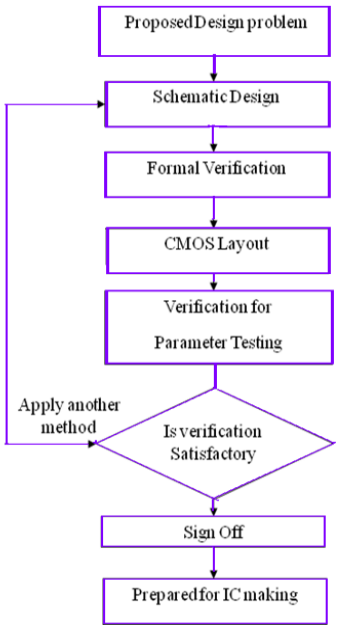


Fig.7.1. Design Flow Chart

To achieve the planned objective following steps are included in the design and analysis of proposed MCAM.

1. Schematic design of proposed MCAM using CMOS transistors.
2. Performance verification of the above for different parameters.
3. CMOS layout for the proposed MCAM using VLSI backend.
4. Verification of CMOS layout and parameter testing.

If the goal is achieved for all proposed parameter including detail verification, sing off for the design & analysis and design will be all set for IC making. If detail confirmation of parameters would not complete then again follow the first step with different methodology.

The operational voltage is usually from 0.8 V to 1.2 V, dependent on the technology variant. In Microwind, it decided to fix VDD at 1.0 V in the cmos 22nm.RUL rule file, which represents a compromise between all possible technology variations available for this 22-nm node.

Effort has been taken to design Low Power, High performance Memristor based Content Addressable Memory (MCAM) cell, using VLSI technology. The design procedure, at various levels, is commonly evolutionary in nature. It starts with a given set of prerequisite. When the necessities are not met, the design has to be enhanced. More simplified view of the VLSI technology consists of several representations, concepts of design, logic circuits, CMOS circuits and physical design. Here for the design with VLSI technology microwind3.1 VLSI Backend software is used. This software allows designing and simulating an integrated circuit at physical description level. The proposed work is designed using 22nm CMOS/VLSI technology in Microwind 3.1software. The main novelties related to the 22nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric.

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VIII. CONCLUSION

The proposed Memory is designed using 22 nm CMOS/VLSI technology with Microwind 3.1. The main novelties related to the 22 nm technology are the high-k gate oxide, metal gate and very low-k interconnect .The Software used in program allows us to design and simulate an integrated circuit at physical description level. The non-volatile characteristic and nanoscaled geometry of the memristor together with its compatibility with CMOS process technology increases the memory cell packing density, decreases power dissipation and delivers for new approaches towards power reduction and management through disabling blocks of MCAM cells without loss of stored data.

The conventional 10T NOR-Type CAM cell has more silicon area as compare to other cells but it has advantage over 6T SRAM cell that it has low power ingestion. 7T NOR-TYPE MCAM CELL and 7T NAND-TYPE MCAM CELL practice memristor to overcome the disadvantage of loss of stored data when power supply is turned 'OFF'. When memristor is used in cell then the input data is put in storage in the memory as it is, even if the supply is OFF until following power supply is turned ON.

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